CFP4-27B4-10D-RX

100 Gb/s CFP4 LR4 Receiver

PRODUCT FEATURES

- Compliant with 100GBASE-LR4
- Support line rates from 103.125 Gbps to 111.81 Gbps
- Integrated LAN WDM ROSA for up to 10 km reach over SMF
- Digital Diagnostics Monitoring Interface
- Duplex LC optical receptacle
- No external reference clock
- Single 3.3 V power supply
- Case operating temperature range:0°C to 70°C
- Power dissipation < 2W

APPLICATIONS

- Data Center &100G Ethernet
- ITU-T OTU4

STANDARD

- Compliant to IEEE 802.3ba
- Compliant to CFP MSA CFP4 Hardware Specification
- Compliant to CFP MSA Management Interface Specification

General Description

XGIGA 100G CFP4 LR4 optical Receiver integrates receiver on one module. In the receive side, the four lanes of optical data streams are optically de-multiplexed by the integrated optical de-multiplexer. Each data stream is recovered by a PIN photo-detector and trans-impedance amplifier, retimed. This module features a hot-pluggable electrical interface, low power consumption and MDIO management interface.

The module provides an aggregated signaling rate from 103.125 Gbps to 111.81 Gbps. It is compliant with IEEE 802.3 ba 100GBASE-LR4 and ITU-T G.959.1, and OIF CEI-28G-VSR. The MDIO management interface complies with IEEE 802.3 Clause 45 standard. The transceiver complies with CFP MSA CFP4 Hardware Specification, CFP MSA Management Interface Specification, and OIF CEI-28G-VSR standards.

Receiver

The receiver takes incoming combined four lanes optical data from line rate of 25.78 Gbps to 27.95 Gbps through an industry standard LC optical connector. The four incoming wavelengths are separated by an optical de-multiplexer into four separated channels. Each output is coupled to a PIN photo-detector. The electrical currents from each PIN photo-detector are converted to a voltage with a high-gain trans-impedance amplifier. The electrical output is recovered and retimed by the CDR chip. The four lanes of reshaped electrical signals are output to RDxp and RDxn pins.

Low Speed Signaling

Low speed signaling is based on low voltage CMOS (LVCMOS) operating at a nominal voltage of 3.3 V for the control and alarm signals, and at a nominal voltage of 1.2 V for MDIO address, clock and data signals. All low speed inputs and outputs are based on the CFP MSA CFP4 Hardware Specification and CFP MSA Management Interface Specification.

MDC/MDIO: Management interface clock and data lines.

GLB_ALEMn: Output pin. When asserted low indicates that the module has detected an alarm condition in any MDIO alarm register.

TX_Disable: Input pin. When asserted high or left open the transmitter output is turned off. When Tx_Dsiable is asserted low or grounded the module transmitter is operating normally. Pulled up with 4.7

kΩ to 10 kΩ resistors to 3.3 V inside the CFP4 module.

MOD_LOPWR: Input pin. When asserted high or left open the CFP4 module is in low power mode. When asserted low or grounded the module is operating normally. Pulled up with 4.7 kΩ to 10 kΩ resistors to 3.3 V inside the CFP4 module.

MOD_RSTn: Input pin. When asserted low or grounded the module is in Reset mode. When asserted high or left open the CFP4 module is operating normally after an initialization process. Pulled down with 4.7 kΩ to 10 kΩ resistors to ground inside the CFP4 module.

Mod_ABS: Output pin. Asserted high when the CFP4 module is absent and is pulled low when the CFP4 module is inserted.

RX_LOS: Output pin. Asserted high when insufficient optical power for reliable signal reception is received.

Pin Function Definitions

Top Raw		Bottom Row	
PIN#	Name	PIN#	Name
56	GND	1	3.3V_GND
55	TX3n	2	3.3V_GND
54	TX3p	3	3.3V
53	GND	4	3.3V
52	TX2n	5	3.3V
51	TX2p	6	3.3V
50	GND	7	3.3V_GND
49	TX1n	8	3.3V_GND
48	TX1p	9	NUC
47	GND	10	NUC
46	TX0n	11	TX_DIS
45	TX0p	12	RX_LOS
44	GND	13	GLB_ALRMn
43	(REFCLKn)	14	MOD_LOPWR
42	(REFCLKp)	15	MOD_ABS
41	GND	16	MOD_RSTn
40	RX3n	17	MDC
39	RX3p	18	MDIO
38	GND	19	PRTADR0
37	RX2n	20	PRTADR1
36	RX2p	21	PRTADR2
35	GND	22	NUC
34	RX1n	23	NUC
33	RX1p	24	NUC
32	GND	25	GND
31	RX0n	26	TX_MCLKn
30	RX0p	27	TX_MCLKp
29	GND	28	GND

Figure 1 CFP4 optical transceiver pin-out

Table 1 CFP4 optical transceiver pin descriptions

Pin no.	Type	Description
1	3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
2	3.3V_GND	
3	3.3V	3.3V Module Supply Voltage
4	3.3V	3.3V Module Supply Voltage
5	3.3V	3.3V Module Supply Voltage
6	3.3V	3.3V Module Supply Voltage
7	3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V_GND	
9	NUC	Module Vendor I/O. Must No Connect at host board
10	NUC	Module Vendor I/O. Must No Connect at host board
11	TX_DIS	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
12	RX_LOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
13	GLB_ALRMn	Global Alarm. “0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
14	MOD_LOPWR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
15	MOD_ABS	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
16	MOD_RSTn	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
17	MDC	Management Data Clock (electrical specs as per 802.3ae and ba)
18	MDIO	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
19	PRTADR0	MDIO Physical Port address bit 0
20	PRTADR1	MDIO Physical Port address bit 1
21	PRTADR2	MDIO Physical Port address bit 2
22	NUC	Module Vendor I/O. Must No Connect at host board
23	NUC	Module Vendor I/O. Must No Connect at host board
24	NUC	Module Vendor I/O. Must No Connect at host board
25	GND	
26	TX_MCLKn	TX Monitor Clock Output (Positive)
27	TX_MCLKp	TX Monitor Clock Output (Negative)
28	GND	

Pin no.	Type	Description
29	GND	
30	RX0p	Lane 0 Receiver Output (Positive)
31	RX0n	Lane 0 Receiver Output (Negative)
32	GND	
33	RX1p	Lane 1 Receiver Output (Positive)
34	RX1n	Lane 1 Receiver Output (Negative)
35	GND	
36	RX2p	Lane 2 Receiver Output (Positive)
37	RX2n	Lane 2 Receiver Output (Negative)
38	GND	
39	RX3p	Lane 3 Receiver Output (Positive)
40	RX3n	Lane 3 Receiver Output (Negative)
41	GND	
42	REFCLKp(NUC)	Reference Clock Input (Positive) (Optional)
43	REFCLKn(NUC)	Reference Clock Input (Negative) (Optional)
44	GND	
45	TX0p	Lane 0 Transmitter Input (Positive)
46	TX0n	Lane 0 Transmitter Input (Negative)
47	GND	
48	TX1p	Lane 1 Transmitter Input (Positive)
49	TX1n	Lane 1 Transmitter Input (Negative)
50	GND	
51	TX2p	Lane 2 Transmitter Input (Positive)
52	TX2n	Lane 2 Transmitter Input (Negative)
53	GND	
54	TX3p	Lane 3 Transmitter Input (Positive)
55	TX3n	Lane 3 Transmitter Input (Negative)
56	GND	

I. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	Ts	-40	-	85	℃	
Relative Humidity	RH	5	-	95	%	
Power Supply Voltage	VCC	-0.3	-	4	V	
Signal Input Voltage		Vcc-0.3	-	Vcc+0.3	V	
Receive Input Optical Power (Damage threshold)	Pdmg			5.0	dBm	

II. Low Speed Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Supply currents and voltages						
Voltage	Vcc	3.2	3.3	3.4	V	With Respect to GND
Supply current	Icc			0.6	A	
Power dissipation	Pwr			2.0	W	
Low speed control and sense signals, 3.3 V LVCMOS						
Outputs low voltage	V_{OL}	-0.3		0.2	V	I_{OH}=100 µA
Output high voltage	V_{OH}	Vcc-0.2		Vcc+0.3	V	I_{OH}=-100 µA
Low speed control and sense signals, 1.2 V LVCMOS						
Outputs low voltage	V_{OL}	-0.3		0.2	V	
Output high voltage	V_{OH}	1.0		1.5	V	
Output low current	I_{OL}	4			mA	
Output high current	I_{OH}			-4	mA	
MDC clock rate		0.1		4	MHz	

III. High Speed Electrical Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Receiver electrical output to host					
Differential voltage pk-pk		100	1200	mV	
Common mode noise (rms)			17.5	mV	
Differential termination mismatch			10	%	
Transition time		9.5		ps	20/80%

IV. MDIO Management Interface

The XGIGA CFP4 Optical Transceiver incorporates MDIO management interface which is used for serial ID, digital diagnostics, and certain control and status report functions. The CFP4 transceiver supports MDIO pages 8000h NVR 1 Based ID registers, 8080h NVR 2 Extended ID registers, 8100h NVR 3 network lane specific registers , 8180h NVR 4 registers ,and pages A000h module VR 1 registers(module level control and DDM registers)， A200h network lane VR 1 registers，A280h network lane VR 2 registers,A400h host lane VR1 specific registers.

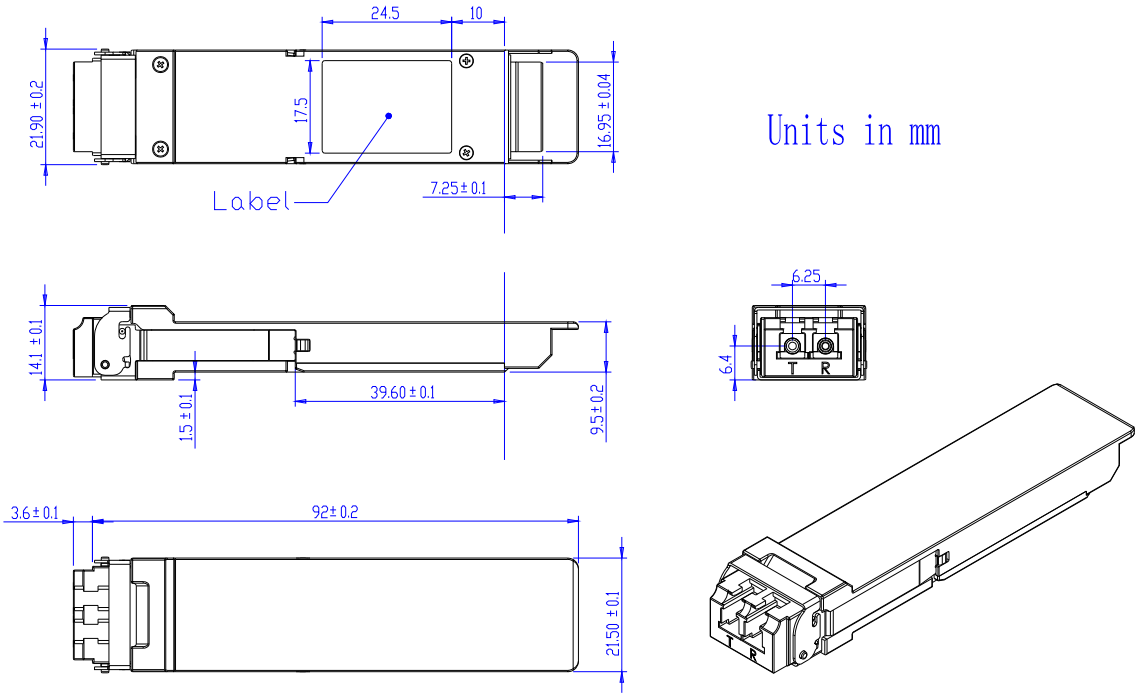
Details of the protocol and interface are explicitly described in CFP MSA Management Interface Specification. Please refer to the specifications for design reference.

V. Optical Receiver Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Signaling rate, each lane			25.78125		Gbps	
Rate tolerance		-100		100	ppm	From normal rate
Average receive power, each lane	Pavg	-10.6		4.5	dBm	
Receive max power, each lane (OMA)				4.5	dBm	
Difference in launch power between any two lanes (OMA)				5.5	dB	
Receiver Sensitivity (OMA), each lane	Rsen			-8.6	dBm	1
Stressed Receiver Sensitivity (OMA), each lane	SRS			-6.8	dBm	
Stressed receiver sensitivity test conditions						
Vertical eye closure penalty, each lane	VECP		1.8		dB	
Stressed sys J2 jitter, each lane	J2		0.3		UI	2
Stressed sys J9 jitter, each lane	J9		0.47		UI	2
Receiver reflectance				-26	dB	
LOS Assert	LOSA	-30			dBm	
LOS De-assert	LOSD			-12	dBm	
LOS Hysteresis		0.5		4	dB	

1. Receiver sensitivity (OMA), each lane, is informative.
2. Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

VI. Outline Dimensions



Appendix A. Document Revision

Version No.	Date	Description
Preliminary	2015-05-04	Preliminary datasheet